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10/812,579	03/29/2004	Sharon Zohar	MAGMA-00702	3216

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EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/812,579	ZOHAR, SHARON	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/26/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication application 10/812,579 filed on 03/29/2004, claims 1-23 are pending.

Drawings

2. Figures 1-5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 7-17, and 19-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Okuzawa et al. (Okuzawa) (US 5,243,538).

5. **With respect to claim 1**, Okuzawa discloses a method (col. 1, ll. 6-10) of designing an integrated circuit comprising programming a processing path within the integrated circuit according to a first substitute circuit (logic circuit) comprising substitute inputs and a substitute output (col. 5, ll. 7-13, and figures 6, --upper and lower level logic has inputs A, B and output Z), wherein a truth table representing the first substitute circuit is identical to a truth table representing a first sequence of Boolean elements representing a processing path (if it is the logic circuit element defined by the Boolean expression) (fig. 9, steps [201], [203], and [205] and col. 5, ll. 56-62; col. 6, ll. 10-33) and wherein the first substitute circuit is not definable by a sequence of basic Boolean circuits (if it is not of the logic circuit element defined by the Boolean expression) (fig. 9, steps [201], [202], [204] and [205] and col. 5, ll. 49-55 and ll. 63-67; col. 6, ll. 1-9).

6. **With respect to claim 2**, Okuzawa discloses the method according to claim 1 further comprising generating the first substitute circuit (logic circuit) (fig. 5, elements [51-54] and col. 10, ll. 1-6; and fig. 8, elements [10, 11]; col. 4, ll. 6-15, ll. 67-68 and col. 5, ll. 1-44, -- extracting data format from Boolean expression of upper and lower logic, then generating logic circuit by given signal name or input/output and module name).

7. **With respect to claim 3**, Okuzawa discloses the method according to claim 2 further comprising receiving (pick up) the first sequence of basic Boolean elements (figure 8, elements [11; 105-105], and col. 10, ll. 1-6, ll. 26-35).

8. **With respect to claim 4**, Okuzawa discloses the method according to claim 1 wherein the processing path further comprises a flip flop at a processing

path input (fig. 6, elements [61, 62] with flip flop [M1] and col. 4, ll. 36-66; and also refer to figure 8, elements [106]).

9. **With respect to claim 5**, Okuzawa discloses the method according to claim 2 further comprising the step of reducing (simplification) the first sequence of Boolean elements into at least one intermediate equivalent circuit prior to the step of generating a first substitute circuit (figures 2-4, reducing steps, figure 6, upper and lower level logic, figure 8, elements [10-12, 104-106], and figure 11, col. 8, ll. 15-34 –simplification step --).

10. **With respect to claim 7**, Okuzawa discloses the method according to claim 3 wherein the first sequence of basic Boolean elements is less than or equal to twenty Boolean operators (figure 6, elements [62, 64], which are less than twenty operators, and col. 7, ll. 20-32, -- the number n variables as same as Boolean operators, if n less than or equal to 21, then it performs less than or equal to 20's Boolean operators --).

11. **With respect to claim 8**, Okuzawa discloses the method according to claim 3 wherein the first sequence of basic Boolean elements comprises a logical sequence greater than twenty Boolean elements (col. 7, ll. 20-32, -- as assumption in claim 7 that the number n variables as same as Boolean operators, and n is greater than 21, then it performs greater than 20's Boolean operators --).

12. **With respect to claim 9**, Okuzawa discloses the method according to claim 3 wherein the step of receiving (pick up)the first sequence of basic Boolean elements (figure 8, elements [11, 104], and col. 10, ll. 1-6, ll. 26-35) precedes

the step of generating a first substitute circuit (figure 8, elements [11, 105]; col. 4, ll. 6-15, ll. 67-68 and col. 5, ll. 1-44, -- extracting data format from Boolean expression of upper and lower logic, then generating logic circuit by given signal name or input/output and module name).

13. **With respect to claim 10**, Okuzawa discloses the method according to claim 1 wherein the step of programming is preceded by the steps:

a. generating a plurality of sequences of basic Boolean elements respectively defined by a plurality of truth tables (figure 9, steps [201, 203,205], col. 5, ll. 56-67 and col. 6, ll. 10-33);

b. generating a respective plurality of substitute circuits not definable by a sequence of basic Boolean elements, including the first substitute circuit, wherein a sequence of basic Boolean elements and its respective substitute circuit are defined by a same truth table (figure 9, steps [201, 202, 204, and 205], col. 5, ll. 48-55 and col. 6, ll. 1-9);

c. storing the plurality of sequences of basic Boolean elements in a library (col. 6, ll. 1-9); and

d. storing the plurality of substitute circuits in the library in a relationship corresponding to their respective sequence of basic Boolean elements (col. 7, ll. 36-59, col. 8, ll. 47-68, and col. 9, ll. 41-48).

14. **With respect to claim 11**, Okuzawa discloses the method according to claim 10 further comprising the steps:

e. receiving a first sequence of basic Boolean elements (figure 8, elements [11, 104], col. 10, ll. 1-6, ll. 26-35, and figure 12, step [501]); and

f. searching the library for the first substitute circuit (figure 12, step [502], col. 9, ll. 1-34).

15. **With respect to claim 12**, Okuzawa discloses the method according to claim 11 further comprising the steps:

a. failing to locate (not found) the first sequence of basic Boolean elements within the library (fig. 9, steps [201 and 202], col. 5, ll. 47-55, and col. 9, ll. 35-40);

b. generating (produce) the first substitute circuit (fig. 9, steps [204], col. 5, ll. 63-68; col. 6, ll. 1-9, and col. 10, ll. 1-6); and

c. adding (storing) the first substitute circuit to the library (fig. 9, steps [204 and 205], col. 6, ll. 4-9 and ll. 28-33).

16. **With respect to claim 13**, Okuzawa discloses the method according to claim 11 wherein the step of receiving the first sequence of basic Boolean elements is followed by the steps:

a. locating (searching) the first sequence of Boolean elements within the library (fig. 9, steps [201 and 203], col. 6, ll. 10-28); and

b. locating (searching) the first substitute circuit within the library corresponding to the first sequence of Boolean elements (fig. 9, steps [203 and 205], col. 6, ll. 28-33).

17. **With respect to claim 14**, Okuzawa discloses the method according to claim 10 wherein the library comprises a digital memory (figure 7, col. 3, ll. 56-63).

18. **With respect to claim 15**, Okuzawa discloses the method according to claim 11 comprising a search engine for searching the library for the first sequence of basic Boolean elements (figure 8, elements [12, 13] and col. 9, ll. .1-34 and figure 12, steps [501-504], col. 9, ll. 40-68).

19. **With respect to claim 16**, Okuzawa discloses an apparatus (figures 7 and 8) for reducing a throughput time of a processing path of basic logic elements within an integrated circuit, the apparatus comprising a programming module for programming (figures 7-8) a first substitute circuit into the processing path of the integrated circuit (Figure 8, --upper and lower level logic files [106a, 106b]), wherein the substitute circuit is not defined by a sequence of basic Boolean circuits (if it is not of the logic circuit element defined by the Boolean expression) (fig. 9, steps [201], [202], [204] and [205] and col. 5, ll. 49-55 and ll. 63-67; col. 6, ll. 1-9), and wherein the substitute circuit is defined by a truth table identical to a truth table defining a processing path comprised of basic Boolean circuits (if it is the logic circuit element defined by the Boolean expression) (fig. 9, steps [201], [203], and [205] and col. 5, ll. 56-62; col. 6, ll. 10-33).

20. **With respect to claim 17**, Okuzawa discloses the apparatus according to claim 16 wherein the processing path comprises an input flip flop (fig. 6, elements [61, 62] with flip flop [M1] and col. 4, ll. 36-66; and also refer to figure 8, elements [106]).

21. **With respect to claim 19**, Okuzawa discloses the apparatus according to claim 16 further comprising a circuit generation module (produce part) (figure 8, element [11]) configured to analyze a sequence of basic Boolean elements and

generate a complimentary substitute circuit (figure 8, elements [11, 104, and 105], and figure 10, col. 7, ll. 10-35).

22. **With respect to claim 20**, Okuzawa discloses the apparatus according to claim 19 further comprising a reduction module (simplification part) configured to reduce a first sequence of Boolean elements into an intermediate circuit sequence (figure 8, element [12], and figure 11, col. 8, ll. 15-36).

23. **With respect to claim 21**, Okuzawa discloses the apparatus according to claim 16 further comprising:

a. a sequence generator for generating a plurality of sequences of Boolean elements (figure 10, col. 7, ll. 10-35), wherein the circuit generation module is configured to generate a complimentary substitute circuit for each sequence of Boolean elements generated (figure 8, elements [11, 104, and 105]);

b. a library for storing the plurality of sequences of Boolean elements such that each Boolean element is stored in a correlation to its complimentary substitute circuit (figure 10A, steps [305-306], and figure 10B-10C, col. 10, ll. 20-32);

c. a search module for searching the library for a first sequence of Boolean elements (figure 12, steps [501-504], col. 9, ll. 40-68); and

d. a retrieval module for retrieving (reading) a substitute circuit from the library (col. 5, ll. 47-50, ll. 65-68, and figure 12, steps [505-506]).

24. **With respect to claim 22**, Okuzawa discloses the apparatus according to claim 21 wherein the library is stored on a digital medium (figure 7, col. 3, ll. 56-63).

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 6, 18, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okuzawa et al. (Okuzawa) (US 5,243,538) in view of Applicant's Admitted Prior Art (AAPA).

27. **With respective to claims 6 and 18**, Okuzawa discloses all the set forth of claims under 35 U.S.C. 102 (b) above.

Okuzawa does not explicitly disclose the integrated circuit is a MOS circuit.

AAPA does disclose the integrated circuit is a MOS circuit (Specification, Background of the Invention section, page 2, ll. 2-5).

It would have been obvious to one of ordinary skill in the art to combine Okuzawa and AAPA for designing and configuring an integrate circuit according to predetermined transistor configurations, such as NAND, NOR, OR, and AND gate (AAPA, figure 1-4 and see the descriptions; Okuzawa, figure 6) for using a

common Boolean gates and transistor in a CMOS circuit, which is well known to those skill in the art (AAPA, Specification, Background of the Invention section, page 2, ll. 2-5).

28. **With respect to claim 23**, Okuzawa discloses a method of programming a processing path (figure 8, col. 4, ll. 5-15) comprising an input flip flop within integrated circuit (figure 6, element [M1], and col. 4, ll. 33-66) comprises:

a. receiving a first sequence of basic Boolean elements (figure 11, step [401]);

b. reducing the first sequence of basic Boolean elements to an equivalent sequence of elements (figure 11, step [402], col. 8, ll. 23-30);

c. generating a substitute circuit from the equivalent sequence of elements (figure 11, steps [403-404], col. 8, ll. 30-34); and

d. programming a processing path within the integrated circuit according to the substitute circuit (figure 7-9) , wherein the substitute circuit is not definable by a sequence of basic Boolean elements (if it is not of the logic circuit element defined by the Boolean expression) (fig. 9, steps [201], [202], [204] and [205] and col. 5, ll. 49-55 and ll. 63-67; col. 6, ll. 1-9), and wherein the substitute circuit is generated to define a truth table that also defines the first sequence of Boolean elements (if it is the logic circuit element defined by the Boolean expression) (fig. 9, steps [201], [203], and [205] and col. 5, ll. 56-62; col. 6, ll. 10-33).

Okuzawa does not explicitly disclose the integrated circuit is a MOS circuit.

AAPA does disclose the integrated circuit is a MOS circuit (Specification, Background of the Invention section, page 2, ll. 2-5).

It would have been obvious to one of ordinary skill in the art to combine Okuzawa and AAPA for designing and configuring an integrate circuit according to predetermined transistor configurations, such as NAND, NOR, OR, and AND gate (AAPA, figure 1-4 and see the descriptions; Okuzawa, figure 6) for using a common Boolean gates and transistor in a CMOS circuit, which is well known to those skill in the art (AAPA, Specification, Background of the Invention section, page 2, ll. 2-5).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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